

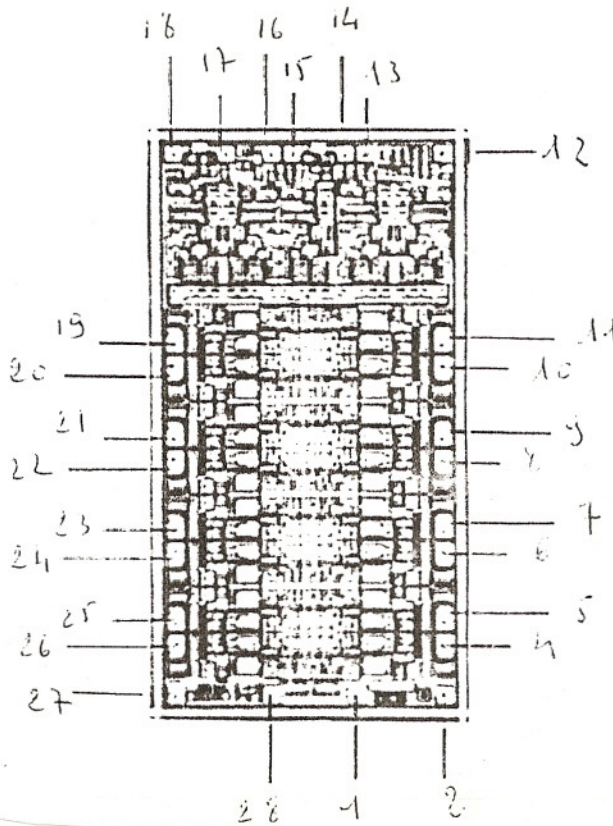


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



## PAD IDENTIFICATION

+VSUPPLY	1	28	OUT A
OUT B	2	27	-VSUPPLY
NC	3	26	IN 8A
IN 8B	4	25	IN 7A
IN 7B	5	24	IN 6A
IN 6B	6	23	IN 5A
IN 5B	7	22	IN 4A
IN 4B	8	21	IN 3A
IN 3B	9	20	IN 2A
IN 2B	10	19	IN 1A
IN 1B	11	18	ENABLE
GND	12	17	ADDRESS A <sub>0</sub>
V <sub>REF</sub>	13	16	ADDRESS A <sub>1</sub>
NC	14	15	ADDRESS A <sub>2</sub>

**Topside Metal: Al**  
**Backside: Si**  
**Backside Potential:**  
**Mask Ref:**  
**Bond Pads : .004 min**

**APPROVED BY: CB**  
**MFG: Harris**

**DIE SIZE: .161" x .084"**  
**THICKNESS: .019"**

**DATE: 2/6/01**  
**P/N: HI547**