# Sierra Components, Inc.

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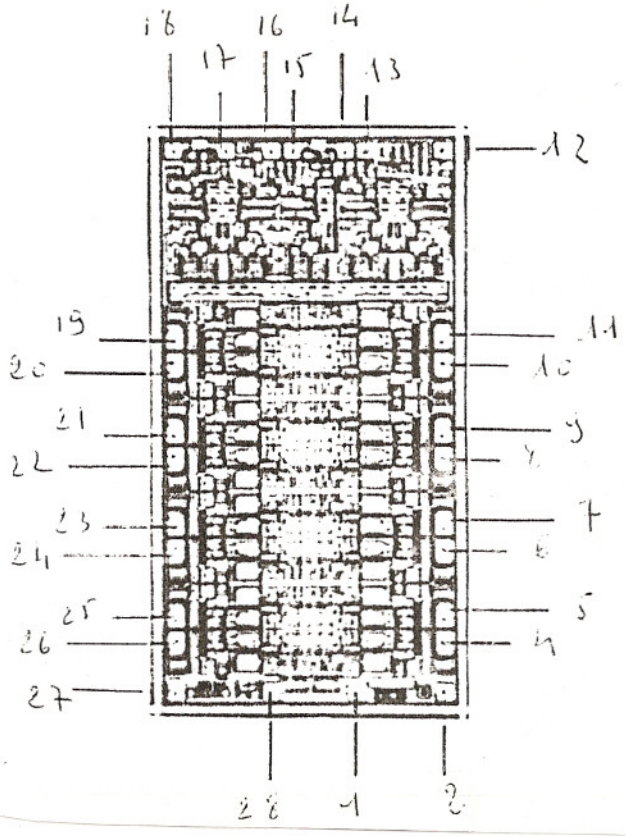
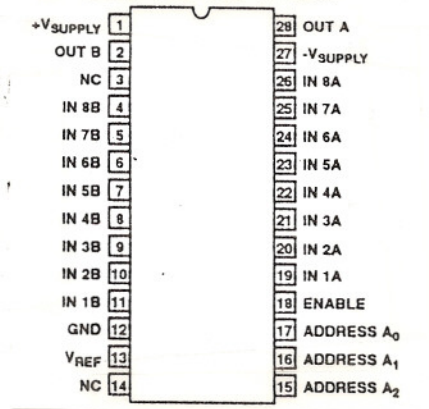
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD IDENTIFICATION




**Topside Metal: Al**
**Backside: Si**
**Backside Potential:**
**Mask Ref:**
**Bond Pads : .004 min**

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|---|---|---|
| **APPROVED BY: CB** | **DIE SIZE: .161" x .084"** | **DATE: 2/6/01** |
| **MFG: Harris** | **THICKNESS: .019"** | **P/N: HI547** |

DG 10.1.2
Rev A 3-4-99